PERICOM

PI6C5930

Low Skew CMOS PLL Clock Driver

Features

- Wide frequency range: 100 MHz max
- Five Q and one Q/2 outputs
- Output skew <250 ps (rising edges)
- Internal RC loop filter network
- Low noise TTL-compatible outputs
- Balanced drive outputs: ±24 mA
- Outputs tri-state and registers reset when OE = LOW
- PLL bypass for testing and low-frequency applications
- Small footprint 20-pin QSOP package (Q)

Description

The PI6C5930 clock driver uses a PLL (phase-locked loop) to reduce time skew between a reference clock input (SYNC) and the outputs. An internal loop filter eliminates the need for external compensation. This driver generates six clock outputs: Q0 through Q4 running at the same frequency, plus Q/2 which runs at one half the frequency of Q0-Q4.

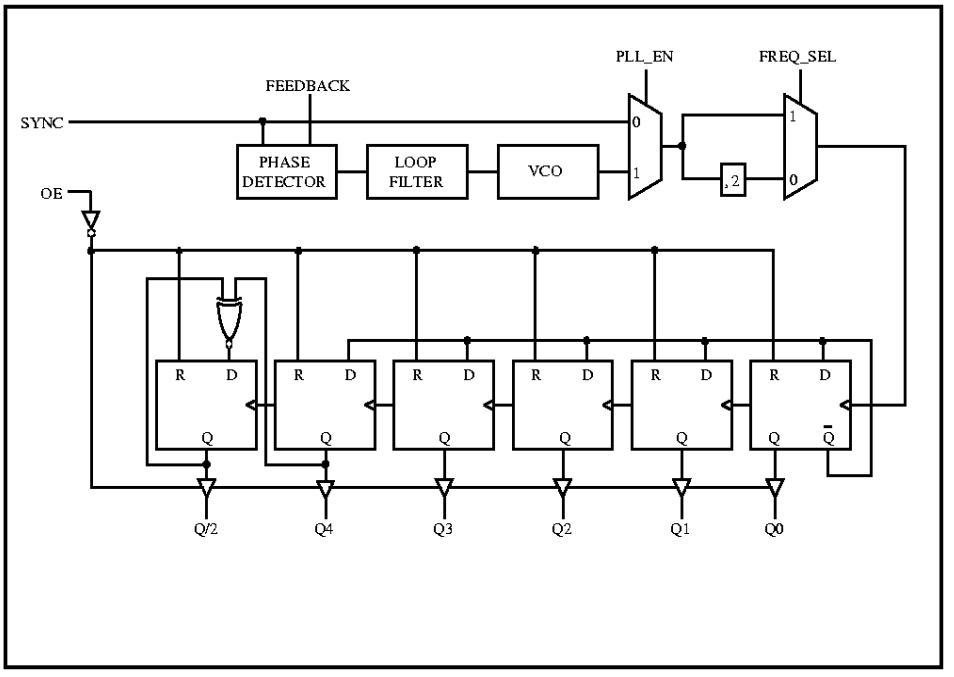
Thanks to design improvements, the PI6C5930 is capable of generating highly stable frequencies up to 100 MHz, while maintaining less than 250 ps skew between outputs.

When FREQ_SEL = HIGH, applying either one of the Q0-Q4 outputs to the FEEDBACK pin results in five copies of the reference input. If Q/2 is applied to the FEEDBACK pin, five clocks at double the reference input are created.

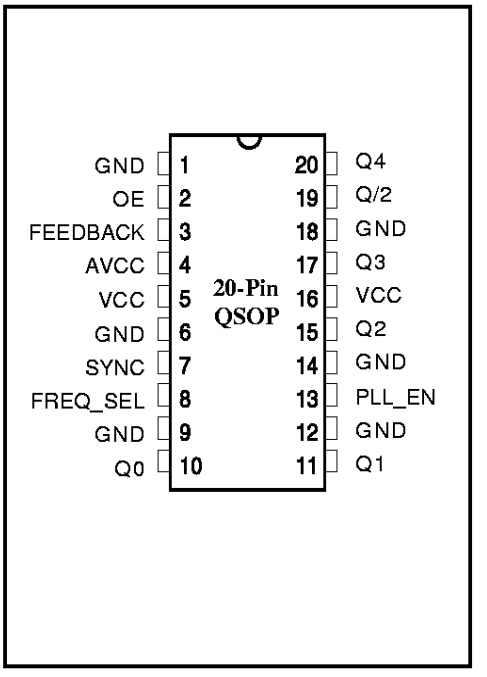
The output enable (OE) function may be used to turn all outputs off and save power. The FREQ_SEL input is set to LOW if the SYNC frequency is lower than 30 MHz, otherwise it should be set HIGH.

The PLL_EN function can be used for testing and to bypass the PLL in low frequency applications.

Block Diagram



Pin Configuration



Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
Maximum Power Dissipation	1.0 W
Storage Temperature	–65°C to +150°C

Note:
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Description

Pin Name	I/O	Functional Description
SYNC	I	Synchronizing Reference Clock Input.
FREQ_SEL	I	Frequency Select. Chooses optimal VCO operating frequency. HIGH is for frequencies >30 MHz, LOW is for frequencies < 30 MHz..
FEEDBACK	I	Feedback Input. Connected to either a Q or a Q/2 output. See the Frequency Selection Table for more information.
Q0-Q4	O	Clock Outputs.
Q/2	O	Clock Output. Synchronized, but runs at half the Q frequency.
OE	I	Output Enable. HIGH = outputs active. LOW = all outputs held in a tri-stated condition and output registers are reset.
PLL_EN	I	PLL Enable. Enables and disables the PLL. When LOW it allows the SYNC input to be passed through for system testing.

Output Frequency Specifications (Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

Symbol	Description	-50	-66	-75	-100	Units
FQ	Maximum frequency, Q0-Q4 outputs	50	66	75	100	MHz
FQ/2	Maximum frequency, Q/2 output	25	33	37.5	50	

Frequency Selection Table

FREQ_SEL	Output Used for Feedback	Allowable SYNC[1] Range (MHz)		Output Frequency Relationships	
		Min	Max	Q Outputs	Q/2
1	Q/2	5	F_Q ÷ 2	SYNC x 2	SYNC
1	Q0-Q4	10	F_Q	SYNC	SYNC ÷ 2
0	Q/2	2.5	F_Q ÷ 4	SYNC x 2	SYNC
0	Q0-Q4	5	F_Q ÷ 2	SYNC	SYNC ÷ 2

Notes:
1. Operation in the specified SYNC frequency range guarantees that the VCO will operate in its optimal frequency range. Operation with SYNC outside the specified frequency ranges may result in invalid or out-of-lock outputs.

DC Electrical Characteristics Over Operating Range (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Conditions	Min	Typ[1]	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	—	—	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –24 mA V_{CC} = Min., I_{OH} = –100 µA	2.4 3.0	2.78 —	— —	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OH} = 24 mA	—	0.21	0.55	V
I_{OZ}	Output Leakage Current	V_{OUT} = V_{CC} or V_{OUT} = GND, V_{CC} = Max., Outputs Disabled	–5	0	5	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or V_{IN} = GND	–5	0	5	µA

Note:
1. Typical values indicate Vcc = 5.0V and T_A = 25°C.

Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]	Typ	Max	Unit
ΔI_{CC}	Input Power Supply Current per TTL Input HIGH	V_{CC} = Max., V_{IN} = 3.4V	0.6	1.5	mA
I_{CCD}	Dynamic Power Supply Current per Output[2]	V_{CC} = Max.	—	0.1	mA/MHz

Notes:
1. For Min. or Max. conditions, use the appropriate values specified under DC specifications,
2. Guaranteed but not tested.
3. For all DC parameters, test conditions assume no output loading.

Input Timing Requirements (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%)

Symbol	Description[1]	Min	Max	Unit
t_R, t_F	Maximum Input Rise and Fall Times, 0.8V to 2.0V	—	3.0	ns
F_I	Input Clock Frequency, SYNC[1]	5	F_Q	MHz
t_{PWC}	Input Clock Pulse, HIGH or LOW	2	—	ns
D_H	Duty Cycle, SYNC	25%	75%	%

Note:
1. The F_I specification is based on Q output feedback. See Frequency Selection Table for more detail on allowable SYNC input frequencies for different feedback combinations.

Capacitance (T_A = 25°C, f = 1 MHz, V_{IN} = 0V, V_{OUT} = 0V)

	QSOP		
Pins	Typ	Max	Unit
C_{IN}	3	4	pF
C_{OUT}	7	9	pF

Note:
Capacitance is characterized but not tested.

Switching Characteristics Over Operating Range

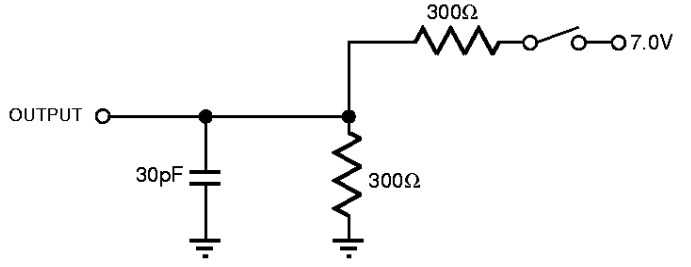
(T_A = 0°C to 70°C, Vcc = 5.0V ± 5%)

Symbol	Description[1]	Min	Typ	Max	Unit
t_{SKR}	Output Skew Between Rising Edges, Q4-Q0 and Q/2[2,3]	—	160	250	ps
t_{SKF}	Output Skew Between Falling Edges, Q4-Q0[2,3]	—	180	500	
t_{PW}	Pulse Width[2]	T_{CY}/2-0.4	—	T_{CY}/2+0.4	ns
t_J	Cycle to Cycle Jitter, 33 MHz[5]	—	100	250	ps
t_{PD}	SYNC Input Feedback Delay, 10 MHz	–300	–204	700	
t_{PD}	SYNC Input Feedback Delay, 33 MHz, 50Ω to 1.5V[2]	–100	—	400	
t_{LOCK}	SYNC to Phase Lock[2]	—	—	10	ms
t_{PZH}, t_{PZL}	Output Enable Time, OE HIGH to Low-Z[4]	0	—	14	ns
t_{PHZ}, t_{PLZ}	Output Disable Time, OE LOW to High-Z[4]	0	—	14	
t_R, t_F	Output Rise and Fall Times, 0.8V to 2.0V[2]	0.5	0.65	1.5	

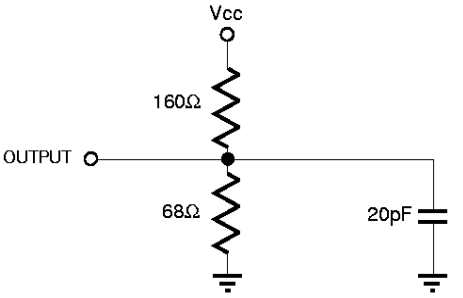
Notes:

1. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2. This parameter is guaranteed by design but not tested.
3. Skew specifications apply under identical environments (loading, temperature, Vcc, device speed grade).
4. Measured in open loop mode PLL_EN = 0.
5. Jitter is characterized using a time interval analyzer. Characterized but not tested. See FREQUENCY SELECTION TABLE for information on proper FREQ_SEL level for specified SYNC input frequencies.

Test Loads

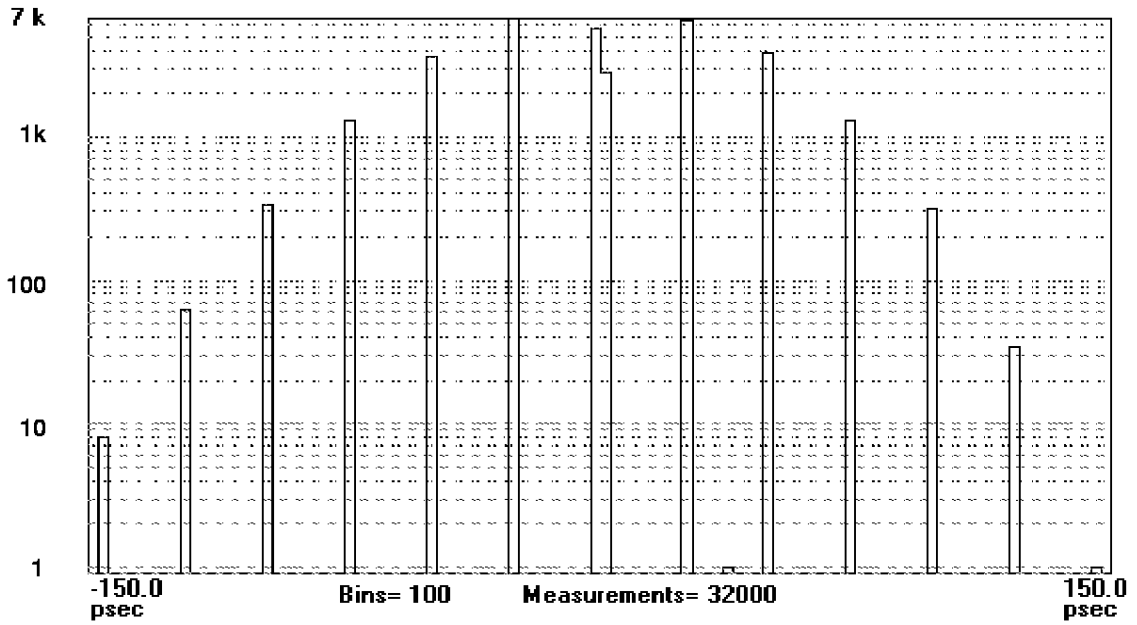


Used for output enable/disable parameters.



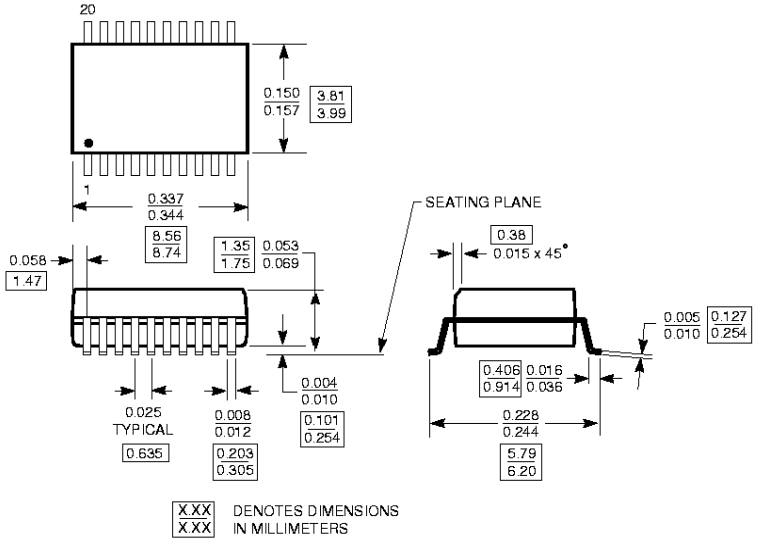
Used for all other timing parameters.

Typical Cycle-to-Cycle Jitter Histogram



Vcc = +4.75V, T_A = 25°C, SYNC = 33 MHz, Q3 output
Fo = 33 MHz, Pace = 2, Population: 32,000
Mean: -1.63, Standard Deviation: 38.88ps

Package Dimensions



Order Information

P/N	Max. Out. Freq.	Pkg.
PI6C5930-50Q	50 MHz	20-pin QSOP
PI6C5930-66Q	66 MHz	
PI6C5930-75Q	75 MHz	
PI6C5930-100Q	100 MHz	

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